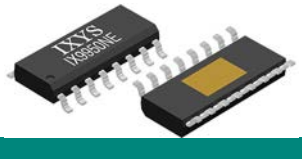
IX9950

110V_{AC} Multi-stage, Dimmable AC Powered LED Driver



Features

- Low additional parts count - one resistor, one low voltage capacitor, and one diode bridge
- No high voltage capacitors or inductors required
- 110V_{AC} Line Powered
- 5-bit Linear Digital Dimming Control
- 0-10V Linear Analog Dimming Control
- Low current distortion
- 0.999 Power Factor
- Excellent current matching (+/- 2.5%)
- Low turn-on voltage
- Current automatically reduced to prevent over temperature failure

Applications

- LED lighting from AC line
- High voltage current regulation

Description

The IX9950 is a multi-stage LED driver that can be used to implement an efficient cost effective LED lighting system without the need for a transformer or inductor. Compared to previous direct AC drive systems, the IX9950 requires fewer external components and has less current distortion resulting in a more linear AC current and a higher power factor than previous stepped current implementations. (US Patents 9,544,961 : 9,924,573 : 9,992,833)

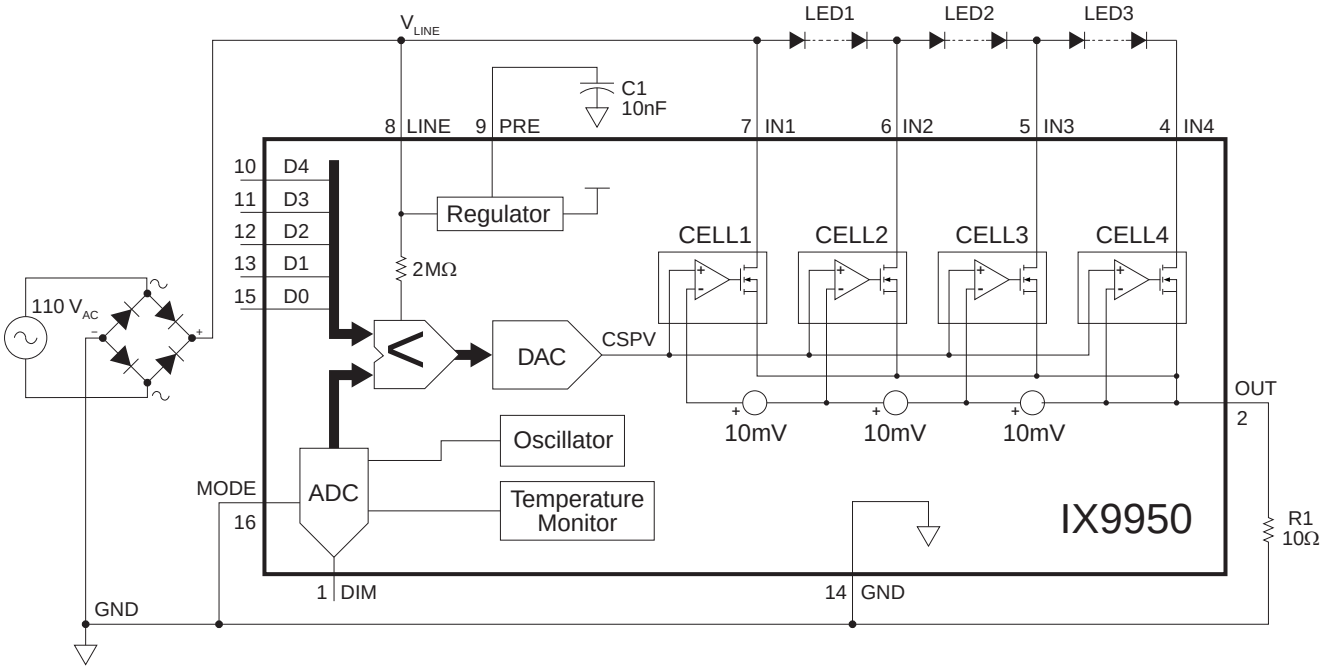
As shown in the Basic Circuit Diagram below, the IX9950 is designed to operate from a 110V_{AC} power source with only a diode bridge, a resistor, and a small low voltage capacitor. Designed to operate with a junction temperature of -40°C to +125°C, the integrated thermal management feature protects the die from thermal damage by reducing the LED current.

The IX9950NE is available in an SOIC(N)-16_EP thermally enhanced 16-pin narrow SOIC package with a bottom side exposed pad.

Ordering Information

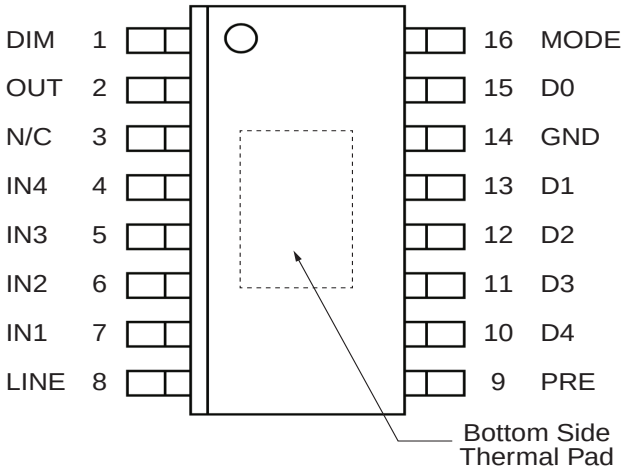
Part	Description
IX9950NE	SOIC(N)-16_EP (50/Tube)
IX9950NETR	SOIC(N)-16_EP Tape & Reel (2000/Reel)

IX9950 Basic Circuit Configuration



1. Specifications

1.1 Package Pinout



1.2 Pin Description

Pin	Name	Description
1	DIM	Analog input: 0V - 10V analog dimming control signal. 10V is full brightness and 0V is off. Internal pull-down, leave open when not used.
2	OUT	Output: Current output for all modules.
3	N/C	Not internally connected
4	IN4	Input: CELL4 current sink terminal.
5	IN3	Input: CELL3 current sink terminal.
6	IN2	Input: CELL2 current sink terminal.
7	IN1	Input: CELL1 current sink terminal.
8	LINE	Power: Provides bias voltage to internal circuitry.
9	PRE	Output: Pre-regulated voltage node for power supply noise reduction capacitor. Recommended value of 10nF.
10	D4	Logic input. D<4:0> MSB used to set brightness in digital dimming mode. Internal pull-up, leave open when not used.
11	D3	Logic input. D<4:0> used to set brightness in digital dimming mode. Internal pull-up, leave open when not used.
12	D2	Logic input. D<4:0> used to set brightness in digital dimming mode. Internal pull-up, leave open when not used.
13	D1	Logic input. D<4:0> LSB used to set brightness in digital dimming mode. Internal pull-up, leave open when not used.
14	GND	Power: Ground
15	D0	Logic input. D<4:0> used to set brightness in digital dimming mode. Internal pull-up, leave open when not used.
16	MODE	Logic input. Dimmer mode selection. Low = Digital dimming: Uses D<4:0> inputs. High = Analog dimming. Uses DIM input. Internal pull-up. Connect to GND when not using built-in dimming functions.
-	Thermal Pad	Thermal pad located on package bottom side. Recommend connecting to GND but may be left floating. Do not connect to any other signal or net. Not intended to carry current

1.3 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
High voltage inputs	V_{LINE}, $V_{IN(1-4)}$	-0.3 to +650	V
DIM voltage	V_{DIM}	-5 to 18	V
Low voltage pins	V_{MODE}, $V_{D<4:0>}$, V_{OUT}	-0.3 to +6	V
Operating junction temperature	T_J	-40 to +125	°C
Storage temperature	T_{STG}	-55 to +125	°C

Electrical absolute maximum ratings are at 25ºC.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Conditions	Symbol	Minimum	Maximum	Unit
High voltage inputs	I_{OUT}=0	V_{LINE}, $V_{IN(1-4)}$	0	570	V
DIM voltage	-	V_{DIM}	0	12	V
Low voltage pins	-	V_{MODE}, $V_{D<4:0>}$, V_{OUT}	0	5.5	V
Regulated cell current					
CELL1	-	I_{IN1}	-	59	mA
CELL2	-	I_{IN2}	-	76	
CELL3	-	I_{IN3}	-	139	
CELL4	-	I_{IN4}	-	217	

1.5 Analog Characteristics

Unless otherwise noted: T_J=-40°C to +125°C; all voltages are with respect to GND.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Unregulated cell current	$V_{IN(1-4)}$ = 25V, V_{OUT} = GND					
CELL1		I_{IN1}	60	111	190	mA
CELL2		I_{IN2}	76	139	238	
CELL3		I_{IN3}	139	252	431	
CELL4		I_{IN4}	217	393	671	
Regulated cell current	V_{MODE}=0V, D<4:0>=OPEN, R1=10Ω					
CELL1	V_{LINE} =20V, V_{IN1}=12V	I_{IN1}	18	20.3	22.5	mA
CELL2	V_{LINE} =50V, V_{IN2}=20V	I_{IN2}	56	58.8	62	
CELL3	V_{LINE} =100V, V_{IN3}=30V	I_{IN3}	118	122	126	
CELL4	V_{LINE} =160V, V_{IN4}=30V	I_{IN4}	196	201	206	
Dimming current regulation	V_{LINE} =160V, V_{IN4}=30V, $V_{IN(1-3)}$=0V, V_{MODE}=0V, R1=10Ω					
	D<4:0>='00001'	$I_{IN4(DIM1)}$	-	6.4	-	mA
	D<4:0>='00011'	$I_{IN4(DIM3)}$	-	19	-	
	D<4:0>='00111'	$I_{IN4(DIM7)}$	-	45	-	
	D<4:0>='01111'	$I_{IN4(DIM15)}$	-	96	-	
Bias current	V_{LINE} = 20V, D<4:0> = MODE=OPEN	I_{LINE}	-	615	-	µA
Shutdown starting temperature	-	-	-	145	-	°C
Shutdown complete temperature	-	-	-	170	-	°C
DIM Pull Down Resistance	-	R_{DIM}	220	300	411	kΩ
LINE input impedance	-	R_{LINE}	-	2	-	MΩ

1.6 Digital Characteristics

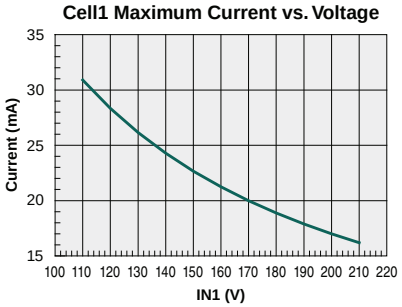
Unless otherwise noted: T_J = -40°C to +125°C; all voltages are with respect to GND.

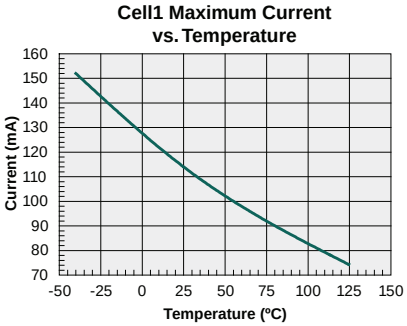
Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Logic Low input voltage threshold	-	V_{LOW}	0.9	1.1	1.4	V
Logic High input voltage threshold	-	V_{HIGH}	1.6	2	2.5	V
Input Hysteresis	-	V_{HYS}	0.7	0.9	1.07	V
Pull-up current	$V_{D<4:0>}$ = V_{MODE} = 0V	$I_{D<4:0>}$, I_{MODE}	4	7	11	µA

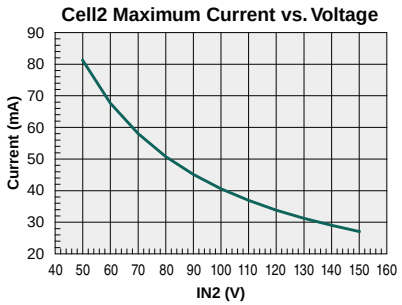
1.7 Thermal Characteristics

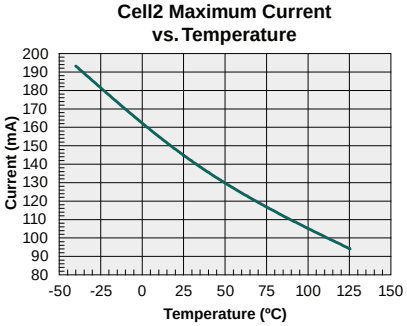
Parameter	Package	Symbol	Rating	Unit
Thermal impedance, junction-to-case	SOIC(N)-16_EP	Θ_{JC}	28	°C/W
Thermal impedance, junction-to-ambient	SOIC(N)-16_EP	Θ_{JA}	60	°C/W

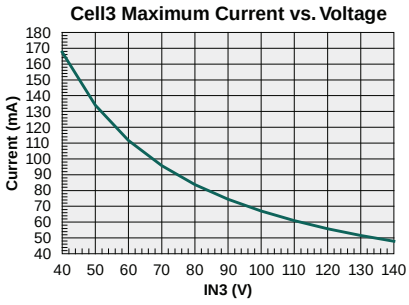
2. Performance Data

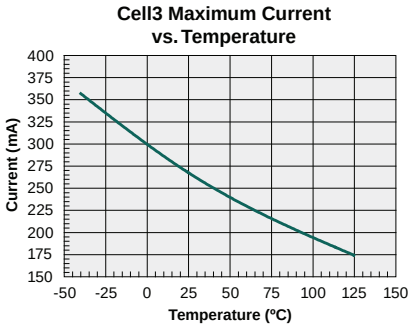


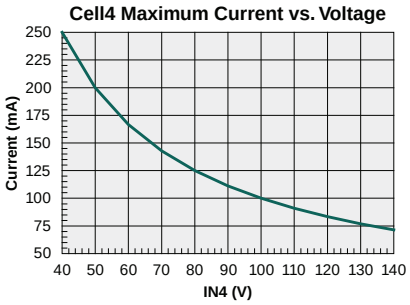


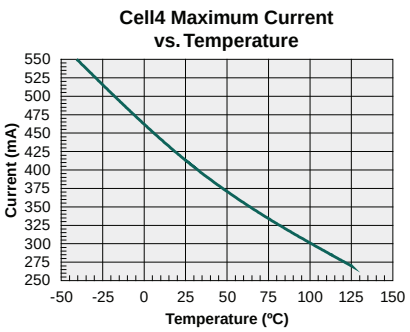


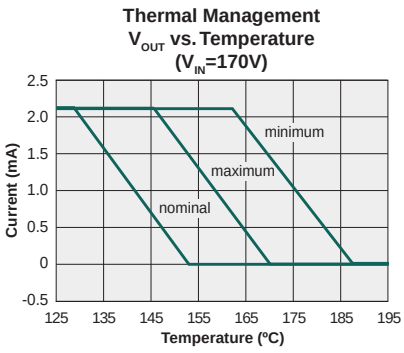












3. Functional Description

3.1 Overview

The IX9950 is a multistage, high-voltage, load current regulating device that can be utilized as an AC line powered LED driver. The intrinsic nature of load current regulators eliminates the need for inductors and capacitors associated with buck and flyback drivers. This architecture facilitates more compact designs with excellent power factor and efficiency ratings while reducing overall bill-of-material (BOM) costs.

The IX9950 is designed to implement a controlled LED sequence with load current regulation where the regulated current value is based on a linear, scaled version of the line voltage. While most AC direct drive devices use multiple resistors with fixed current steps to approximate a sinusoidal load current, the IX9950 produces a nearly perfect sine wave current response with just a single external resistor.

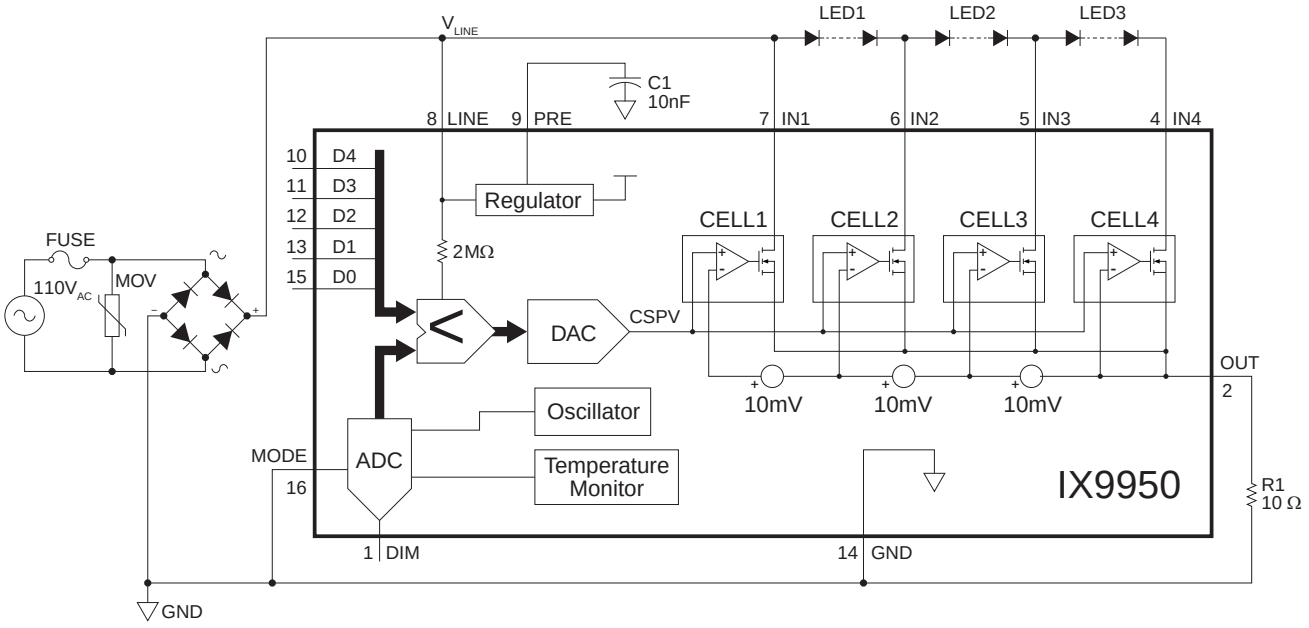
Scaling the LINE input voltage by a factor of 1/80 for a 110V line, the IX9950 creates CSPV, the Current Set Point Voltage. CSPV is used to regulate the current into IN1 and through the LED strings connected to inputs IN2, IN3 and IN4. Each of the four current regulation stages will try to drive sufficient current to the OUT pin so that the output voltage (V_{OUT}) is equal to the CSPV voltage minus the sum of offset voltages in the cell's feedback path.

3.2 Block Diagram

As shown below in the Typical Application Waveforms Over A One-Half AC Cycle, the IX9950 block diagram contains:

- A Regulator to supply low voltage power to the internal circuitry.
- A 5-bit Analog-to-Digital Converter (ADC) to convert the analog dimming control voltage (DIM) to a digital value.
- A parallel 5-bit digital port for digital dimming control.
- A "<" (Less than) logic block to select the lesser of the ADC output or the D<4:0> inputs.
- A 5-bit Digital-to-Analog Converter (DAC) to convert the digital dimming control value to the analog reference voltage used to regulate the current through the cells.
- Four current regulation stages, CELL(1-4) sequentially control the current through the LED strings.
- Three 10mV offset generators to ensure higher current cells disable lower current cells.
- An Oscillator to facilitate ADC operability.
- A Temperature Monitor block to automatically reduce cell current starting at 146°C to prevent over heating.

Figure 1 Typical Application Circuit Without Dimming



3.3 CELL Sequencing

Within the IX9950 are four current regulating stages, CELL(1-4). When powered up, these cells conduct whenever voltage is applied to their IN inputs and their feedback voltage is less than CSPV. All four modules behave in much the same way; they differ in their maximum current sinking ability and the offset voltage between the OUT pin and their amplifier's feedback input.

In a typical application, voltage is applied to IN1 through IN4 sequentially when the voltage applied to the LINE input (V_{LINE}) increases from 0V. Voltage is first applied to the LINE and IN1 inputs. All bias current to operate the internal circuitry is sourced from the LINE input and flows to the GND pin. No bias current is derived from the IN(1-4) pins. When V_{LINE} is high enough for the regulator to power up the internal analog and digital circuits, the CSPV reference voltage will be applied to the current regulation amplifier of each cell.

With the CSPV reference voltage applied to the CELL(1-4) amplifiers, it is compared to the output voltage, $V_{OUT,}$ less the sum of the 10mV offset voltages in the feedback path. Whenever the feedback voltage is less than CSPV, the amplifiers will turn on their high voltage FETs causing load current or additional load current to flow. As the voltage applied to the LINE input increases, CSPV will increase and the amplifiers will respond by increasing the load current to the OUT pin until the amplifier's feedback voltage is equal to CSPV. Higher current cells will drive the feedback voltage of lower current cells above CSPV causing the lower current cells to cease conducting current to the output.

With a falling LINE voltage, CSPV will decrease causing the active current stage to reduce it's current to the OUT pin. This will cause the output voltage and the cell's feedback signal to decrease. As V_{LINE} continues to decrease, the next lower current cell will begin to conduct prior to deactivation of the higher current cell providing a clean decreasing transition.

The offset voltages in the regulation amplifiers feedback path provide the means to assure proper sequencing and current transition from one stage to the next for both the rising and falling sides of the full wave rectified AC input voltage.

3.3.1 LINE Voltage Rising

As can be seen in **Figure 1 "Typical Application Circuit Without Dimming" on page 7**, the voltage applied to the LINE input, $V_{LINE,}$ is also applied directly to IN1. Whenever adequate voltage is applied to the LINE input, the internal circuitry will power up and CELL1 will begin drawing current into IN1. With sufficient voltage at IN1, CELL1 will drive the current necessary for V_{OUT} to track CSPV-30mV.

When V_{LINE} increases to the point where it is larger than the voltage drop across the LED1 string, voltage will commence being applied to IN2 and CELL2 will begin conducting. If V_{IN2}, the voltage applied to IN2, is inadequate, the current through CELL2 will not be sufficient for CELL2 to start regulating. Under this condition, unregulated cell current is limited by the impedance of the LEDs, the resistance of the high voltage FET, and R1. As V_{IN2} increases, CELL2 will begin regulating its current and V_{OUT} will start tracking CSPV-20mV.

When V_{LINE} increases to the point that it is larger than the voltage drop across both the LED1 and LED2 strings, voltage will begin to be applied to IN3 and CELL3 will begin conducting. If V_{IN3}, the voltage applied to IN3, is not large enough, unregulated current will flow through CELL3. Unregulated cell current is limited by the impedance of the LEDs, the resistance of the high voltage FET, and R1. As V_{IN3} increases, CELL3 will begin regulating its current and V_{OUT} will start tracking CSPV-10mV.

When V_{LINE} increases to the point that it is larger than the voltage drop across the LED1, LED2, and LED3 strings, voltage will begin to be applied to IN4 and CELL4 will begin conducting. If $V_{IN4,}$ the voltage applied to IN4, is not large enough, unregulated current will flow through CELL4. Unregulated cell current is limited by the impedance of the LEDs, the resistance of the high voltage FET, and R1. As V_{IN4} increases, CELL4 will begin regulating its current and V_{OUT} will begin tracking CSPV.

3.3.2 Offset Voltages

The 10mV offsets, one each between adjacent cells, in the feedback signal paths from the OUT pin to the current regulation amplifier's inputs ensure active higher current cells automatically disable the current drive capability of the lower current cells. CELL1 with a total offset of 30mV is the lowest current cell and CELL4 with 0mV of offset is the highest current cell.

As V_{LINE} increases, CSPV also increases forcing the next higher current cell to activate which supplements the current to the OUT pin, causing V_{OUT} to rise. When the higher current cell achieves regulation, the output voltage plus the sum of the offsets to the feedback input of the lower current cell will exceed CSPV by 10mV thereby disabling the output current drive of the lower current cell.

For example: If CSPV is 1V then CELL2 will drive V_{OUT} to 0.98V (1V-20mV). When in regulation, the CELL2 amplifier will see 1V at its negative input because there is a 20mV offset in its feedback path. CELL1 however, will see 1.01V (0.98V+30mV) at its negative input and will completely shut down it's output current.

The cells sequential turn-on and automatic turn-off of lower current cells can be seen in Figure 4 on page 12.

In general, whenever V_{OUT} increases due to a higher current cell turning on, the offset will disable the lower current stage. Turning off the lower current cells is important because if they do not shut down, the voltage at their inputs will continue to rise which in turn will increase the power dissipation within their high voltage FETs to excessive levels.

3.3.3 LINE Voltage Falling

For the falling portion of the cycle, when V_{LINE} decreases to the point where there is inadequate voltage applied to IN4 for CELL4 to remain in regulation, the output current drawn from IN4 will begin ramping down. This will cause the output voltage to be reduced to the point that CELL3 will begin to turn back on. The succession of higher current cells dropping out of regulation due to insufficient input voltage and lower current cells becoming active will continue until V_{LINE} drops below the minimum voltage required for operation. To view the current sequence see the waveforms illustrated in Figure 4 on page 12.

For example: If CSPV is 1V and the voltage applied to IN4 is large enough, CELL4 will source sufficient output current so that V_{OUT} is 1V. At this point, the feedback voltage applied to CELL3 is 1.01V, so it is off. CELL2 feedback is 1.02V and CELL1 feedback is 1.03, so they too are off. When the voltage applied to IN4 decreases to the point where CELL4 can no longer source adequate output current to sustain V_{OUT} = 1V, the output voltage will begin falling. As V_{OUT} drops below 0.99V, CELL3 will see its feedback voltage fall below CSPV and will turn on.

3.4 Load Current Calculation

In general, whenever a single cell is providing all of the output current and the current is in regulation, the output voltage is equal to the reference voltage, CSPV, less any offset voltage in the cell's feedback path. Because CSPV is a scaled version of the LINE voltage, whenever the output current is in regulation, V_{OUT} is also a scaled version of the LINE voltage. Since the output current is the output voltage divided by the output resistor, $I_{OUT} = \frac{V_{OUT}}{R}$. and

$$V_{OUT} = CSPV - \Sigma V_{OFFSETS}$$

I_{OUT} is calculated as follows:

$$I_{OUT} = \frac{V_{LINE} - 1.4}{80R} - \frac{\Sigma V_{OFFSETS}}{R}$$

where $CSPV = \frac{V_{LINE} - 1.4}{80}$

In the example below, the output current with a peak AC line voltage of 160V and assuming the rectifier voltage drop is 1.8V, the peak current of CELL4 would be calculated as:

$$I_{OUT} = \frac{V_{LINE} - 1.4}{80R}$$

Setting the output resistor to 10Ω gives a value of:

$$I_{OUT} = \frac{160 - 1.8 - 1.4}{80 \times 10} = \frac{156.8}{800} = 196mA_P$$

The output current is approximately 139mA_{RMS}.

3.5 Dimming

The IX9950 provides 0-10V analog or 5-bit digital dimming control. Configuration of the MODE input allows the user to select either the digital mode, the analog mode, or no dimming. Dimming is implemented by reducing the CSPV voltage applied to the CELLs. Both the digital D<4:0> code and the ADC output code are applied to the Less Than, “<“, block and whichever code is smaller, is passed to the DAC. Whenever MODE is low, it overrides the ADC code representing the analog voltage applied to the DIM input and sets the ADC code for maximum LED current.

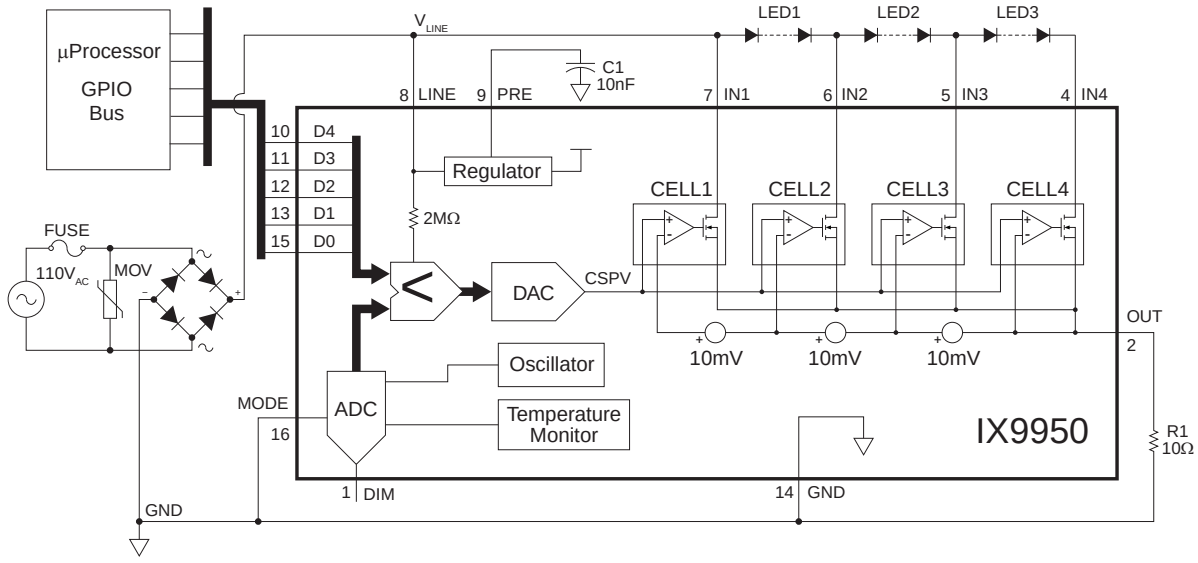
3.5.1 No Dimming

As can be seen in **Figure 1 “Typical Application Circuit Without Dimming” on page 7**, the schematic shows the IX9950 is configured without dimming by tying the MODE input to GND and leaving the DIM and D<4:0> inputs open (floating). Internal pull up resistors on the D<4:0> inputs and an internal pull down on the DIM input secure the inputs to a known state. With MODE pulled low and the D<4:0> inputs pulled high, the IX9950 is set for maximum brightness.

3.5.2 Digital Dimming

Figure 2 shows how to configure the IX9950 for digital dimming. Connecting the MODE pin to GND disables the DIM analog input making it possible to control dimming using the digital D<4:0> inputs. Driving the D<4:0> inputs using a microcontroller or other logic device, a binary code from '11111' to '00000' can be sent to the IX9950 to linearly sweep the LED brightness from maximum to minimum by scaling the CSPV voltage. Since the human eye does not sense brightness linearly, the user may wish to implement a non-linear digital dimming sequence.

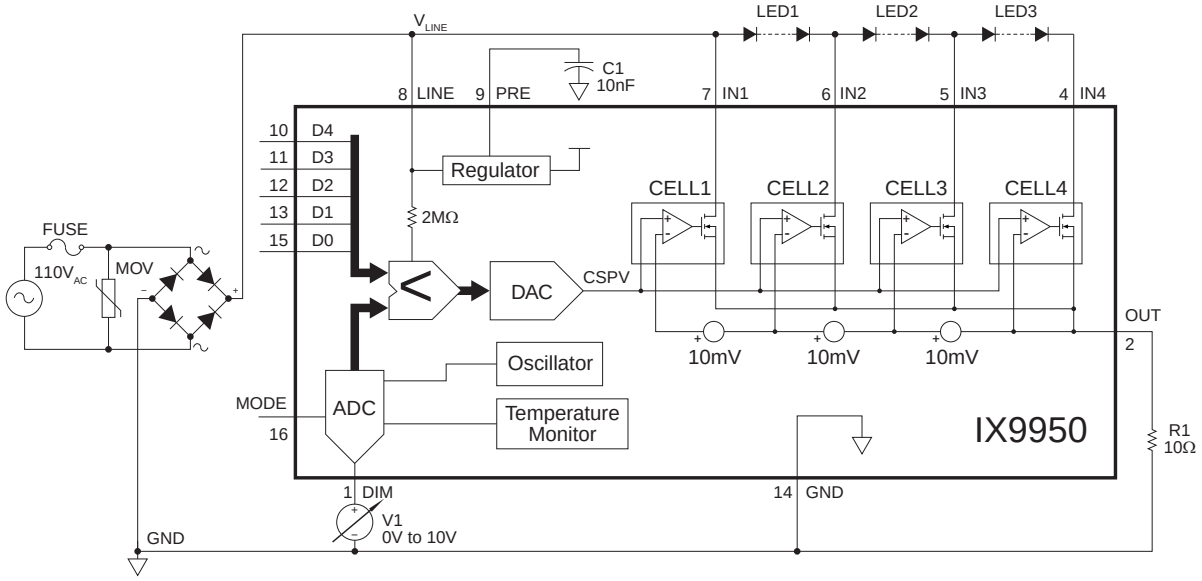
Figure 2 Typical Application with Digital Dimming



3.5.3 Analog Dimming

Figure 3 shows how to configure the device for analog dimming. The MODE and D<4:0> inputs are left floating (open) and a 10V to 0V signal is applied the DIM input to vary the brightness from maximum to minimum. The DIM input voltage is converted by the ADC to a 5-bit code that is used to linearly sweep the LED brightness by scaling the CSPV voltage. Since the human eye does not sense brightness linearly, the user may wish to implement a non-linear DIM control.

Figure 3 Typical Application with Analog Dimming



3.5.4 Dimming Circuit Configurations Summary

Dimming is implemented by the proper conditioning and driving of the MODE, DIM and D<4:0> inputs.

No Dimming

- MODE = GND
- DIM = Open
- D<4:0> = Open

Digital Dimming

- MODE = GND
- DIM = Open
- D<4:0> = Driven from <11111> to <00000>

Analog Dimming

- MODE = Open
- DIM = Driven from 10V to 0V
- D<4:0> = Open

3.6 Thermal Management

Over-temperature thermal management functions in all three dimming modes. At approximately 146°C, the onboard Temperature Monitor senses the die temperature is too high and outputs a current to the ADC that decreases the digital code sent to the "<" comparator. As the temperature rises, the Temperature Monitor current to the ADC will increase causing the ADC output code to decrease.

When the ADC output code falls below the D<4:0> value, the DAC CSPV will decrease which reduces the load current through the device. If the device continues to heat up, the ADC code will reach 0 by approximately 170°C. When a 0 code is applied to the DAC it will reduce the CSPV output to 0V, disabling the cells. With the cells disabled, no current will flow and the device will be protected from over heating.

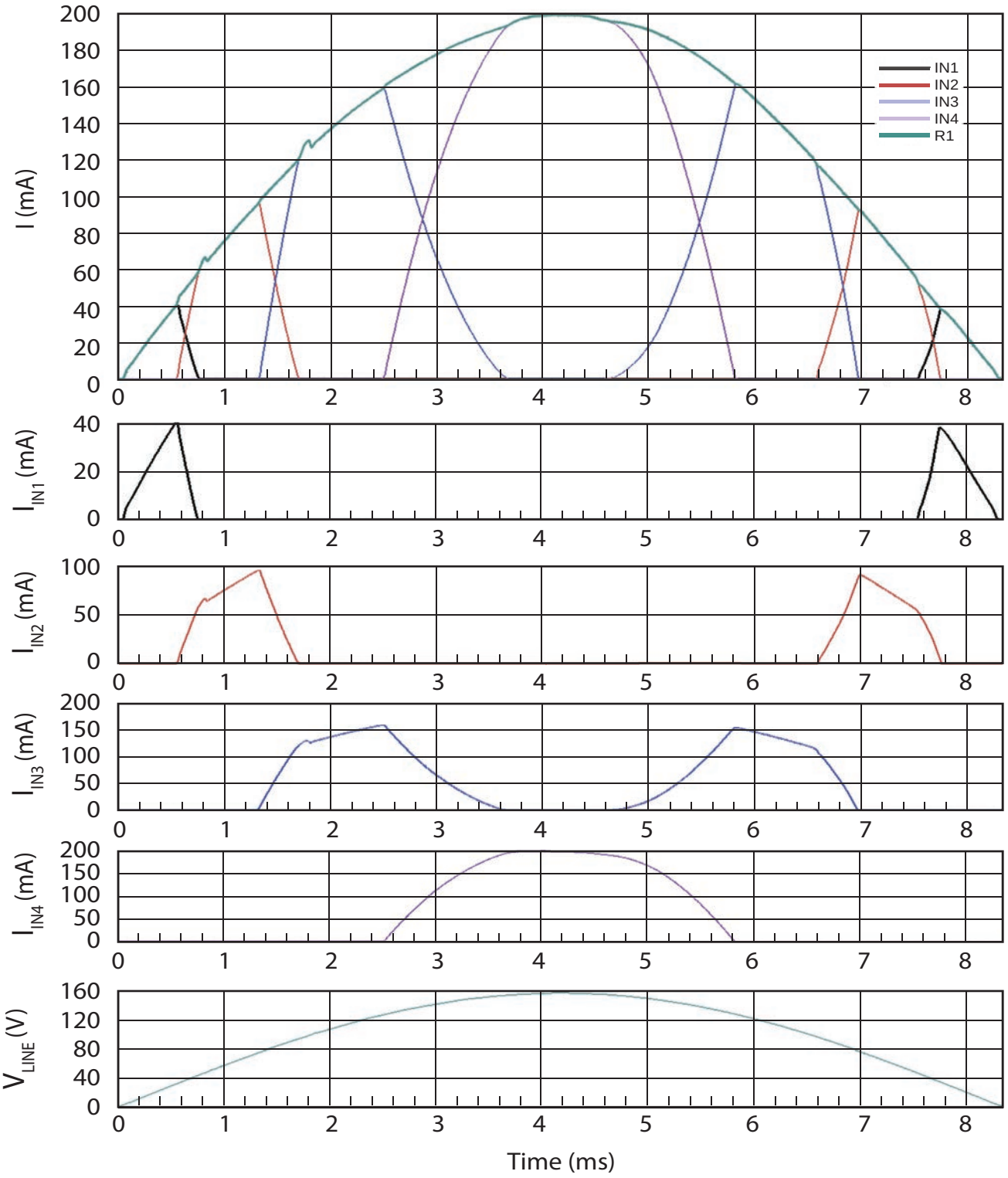
As the die temperature falls, the ADC code will increase and normal operation will return.

3.7 Design Considerations

Pre-regulator filter capacitor: The maximum PRE output voltage at pin 9 is just under 14.5V so the capacitor will need to provide approximately 10nF when biased to this potential.

The digital logic inputs of D<4:0> are internally pulled up to a nominal 4.8V internally generated voltage supply having a maximum level of 5V. Logic devices driving these inputs need to be 5V tolerant.

Figure 4 Typical Application Waveforms Over A One-Half AC Cycle



4. Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX9950NE	MSL 1

4.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes..

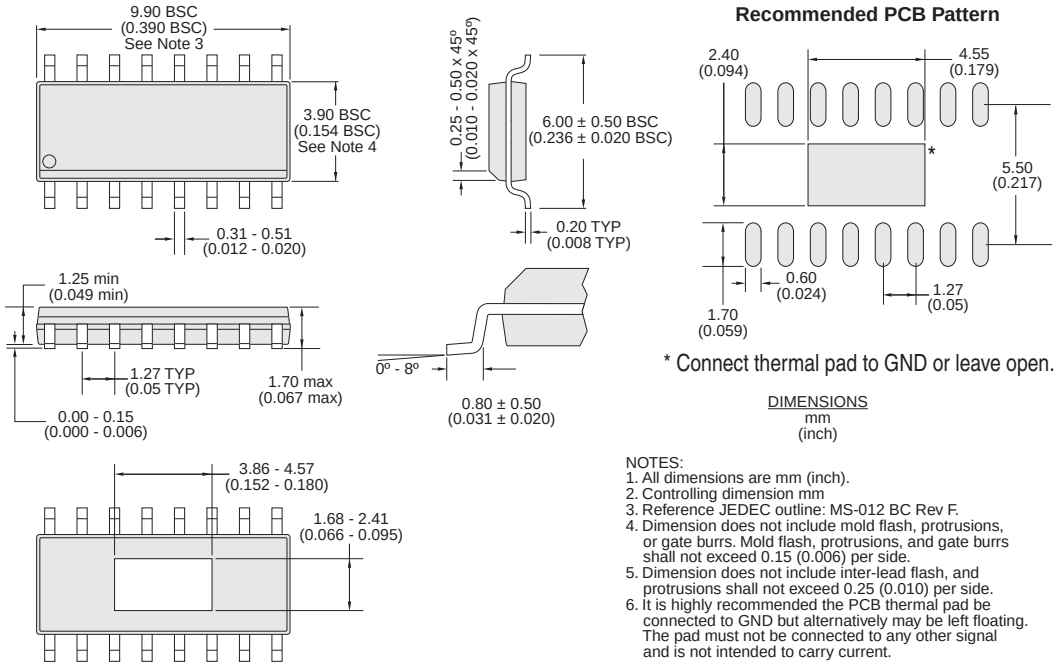
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX9950NE	260°C	30 seconds	3

4.4 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

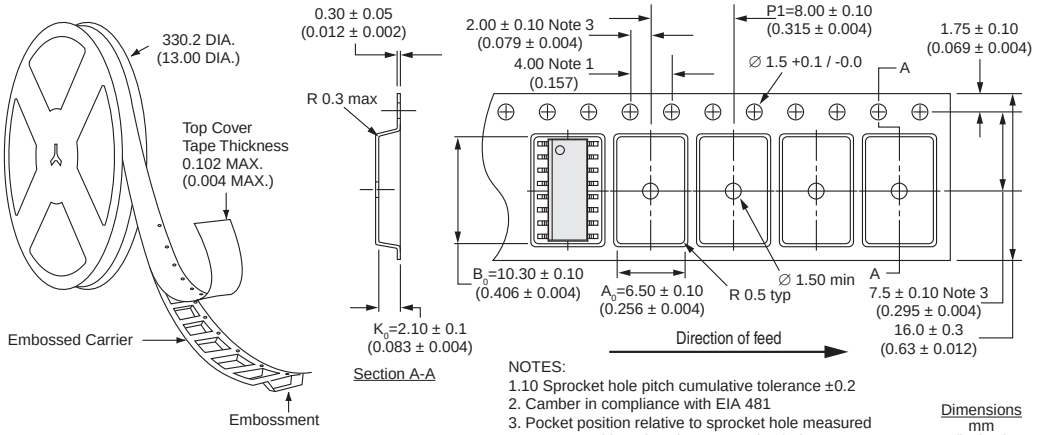
4.5 Mechanical Dimensions

4.5.1 IX9950NE Package



NOTES:
1. All dimensions are mm (inch).
2. Controlling dimension mm
3. Reference JEDEC outline: MS-012 BC Rev F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 (0.006) per side.
5. Dimension does not include inter-lead flash, and protrusions shall not exceed 0.25 (0.010) per side.
6. It is highly recommended the PCB thermal pad be connected to GND but alternatively may be left floating. The pad must not be connected to any other signal and is not intended to carry current.

4.5.2 IX9950NETR Tape & Reel Specification



NOTES:
1.10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions
mm
(inches)

For additional information please visit our website at: https://www.ixysic.com

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