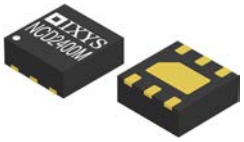
IXYS
INTEGRATED CIRCUITS DIVISION



NCD2400M

Wide Capacitance Range, Non-volatile Digital Programmable Capacitor

PRELIMINARY

Features

- 2-wire (I^2C compatible) serial interface
- 9-bit 512-state digital programmable capacitor
- C_{shunt} = 12.5pF to 194pF (15.6:1 tuning ratio) in discrete 355fF steps
- C_{series} = 1.7pF to 194pF in discrete 376fF steps
- Wide power supply range (2.5 to 5.5V)
- EEPROM non-volatile memory
- Series or shunt configuration supported
- Operation at 105ºC
- 2 x 2 x 0.65 mm 6-pin DFN package, MSL 1

Applications

- OCXOs

Description

The NCD2400M is a dedicated electronic calibrator for oscillators, with reliable performance at 105ºC as required by OCXO applications.

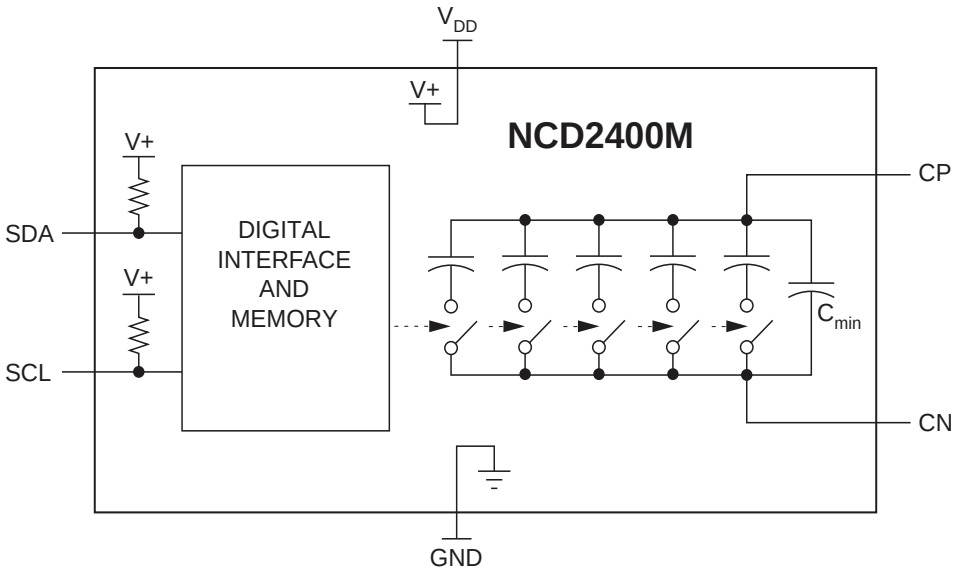
This product can be used in series or shunt configuration, to support a wide variety of tuning circuit topologies.

Digitally controlled capacitance trimming information is communicated via a 2-wire (I^2C compatible) interface. The calibration value can be stored in the internal, re-programmable, non-volatile memory.

Ordering Information

Part #	Description
NCD2400MTR	DFN-6 in Tape & Reel (3000/Reel)

Figure 1. NCD2400M Block Diagram



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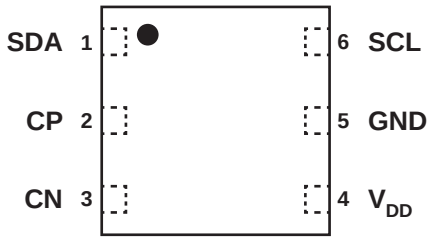
1. Specifications

1.1 Package Pinout



1.2 Pin Descriptions

Pin	Name	Description
1	SDA	Serial interface data
2	CP	Positive capacitance node
3	CN	Negative capacitance node
4	V_{DD}	Power Supply
5	GND	Ground
6	SCL	Serial interface clock

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}-GND	-0.3	+ 6	V
Pins SDA, SCL	GND-0.3	V_{DD} + 0.3	V
Operating Temperature, T_A	-40	+105	°C
Storage Temperature, T_{STG}	-55	+125	°C

Absolute maximum electrical ratings are over the operating temperature range.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply voltage					
Normal operation & shift register mode	V_{DD}	2.5	3.3	5.5	V
Programming & configuration mode		2.5	3.3	5.5	
Operating voltage (1)					
CP to CN	V_{AC}	0	-	3.6	V_{PK}
CP or CN to GND		0	-	3.6 (2)	V_{PK}
CP or CN to GND	V_{DC}	0	-	3.6 (2)	V
Programming time	t_{PV}	4	5	8	ms
Operating temperature					
Normal operation	T_A	- 40	-	+105	°C
Write non-volatile memory operation		- 40	-	+105	

Note 1:V_{DC}+V_{AC} should never exceed 3.6V in operation, and it should never be below 0V.
Note 2:These values should not exceed the supply voltage; e.g. the maximum voltage drop between CN and GND is 2.5V when V_{DD} = 2.5V

1.5 ESD Ratings

Parameter	Symbol	Conditions	Rating	Unit
Human body model	HBM	EIA/JESD22-A114-D All pins except CP and CN	±2	kV
Charged device model	CDM	EIA/JESD22-C101-C All pins except CP and CN	±500	V

1.6 General Conditions for Electrical Characteristics

Typical values are characteristic of the device and are the result of engineering evaluations. They are provided for informational purposes only, and are not guaranteed by production testing.

Unless otherwise specified, specifications cover the operating temperature range T_A=-40ºC to +105ºC and the supply voltage range V_{DD}= 2.5V to 5.5V.

1.7 Capacitor Electrical Characteristics

Expected performance at the nominal operating temperature of 25±5°C and CP and CN terminals biased at half of the supply voltage, unless otherwise noted.

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency range	-	-	0.2	-	150	MHz
Minimum capacitance	Series, Code=0, f=10MHz,	$C_{min10MHz}$	1.6	1.7	1.9	pF
Maximum capacitance	Series, Code=511, f=10MHz,	$C_{max10MHz}$	177.3	194	209.2	
Minimum capacitance	Series, Code=0, f=50MHz,	$C_{min50MHz}$	1.6	1.7	1.9	
Maximum capacitance	Series, Code=511, f=50MHz,	$C_{max50MHz}$	183.3	202.2	219.5	
Tuning ratio (shunt configuration)	C_{max} / C_{min}, f=10MHz	-	-	15.6:1	-	-
Step size	Constant step size at f=10MHz	C_{step}	-	367	-	fF
Quality factor C_{min}	10MHz	$QC_{min10MHz}$	-	>150	-	-
Quality factor C_{max}	10MHz	$QC_{max10MHz}$	35	95	-	-
Quality factor C_{min}	50MHz	$QC_{min50MHz}$	-	43	-	-
Quality factor C_{max}	50MHz	$QC_{max50MHz}$	6.6	18.5	-	-
Capacitance variation with temperature	Local temperature coefficient, in the range - 40°C to +105°C, f=10MHz	C_{ppmT}	-	250	680	ppm/°C

1.8 Power Supply

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD}	2.5	3.3	5.5	V
Supply current	I_{DD}	-	50	90	µA

2. Performance Data

Note: the performance data shown in the graphs below is the measured performance at ambient temperature.

The shunt and series capacitances, in pF, are expected to vary as indicated in the following equations:

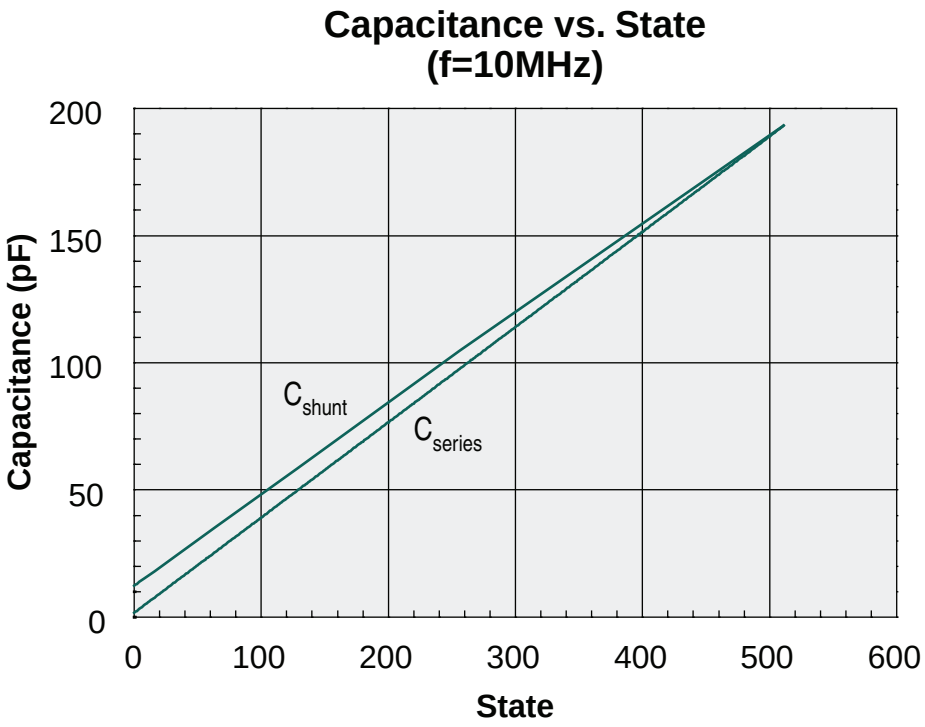
$$C_{SHUNT} = (0.355 \bullet (2^n - 1)) + 12.5$$

$$C_{SERIES} = (0.376 \bullet (2^n - 1)) + 1.7$$

Where n = 0 to 8.

Other aspects of the expected behavior of the tunable capacitor are exemplified in the graphs below.

Figure 1: Shunt and Series Capacitance vs. Code



In shunt configuration, the parasitic capacitance of the package from the CP pin to GND adds up to the total equivalent capacitance of the device. The expected values are the ones defined by the above equation. In series configuration, though, this parasitic capacitor is not part of the equivalent impedance of the device, therefore the overall capacitance seen between CP and CN is smaller.

Figure 2: Series Capacitance vs. Frequency for Selected Codes

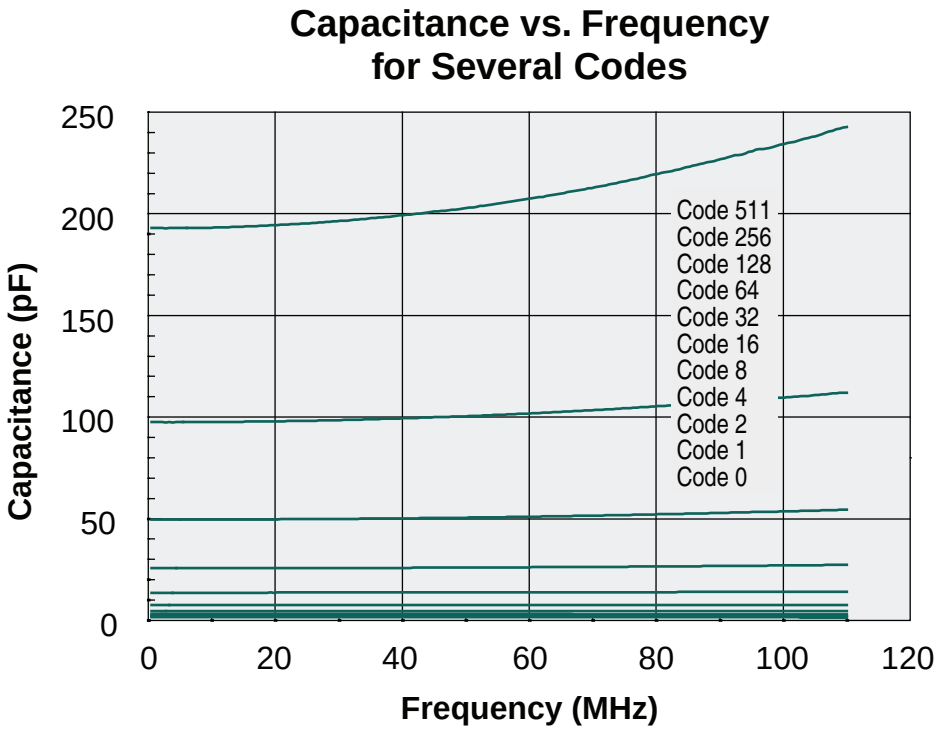


Figure 3: Quality Factor vs. Frequency and Code

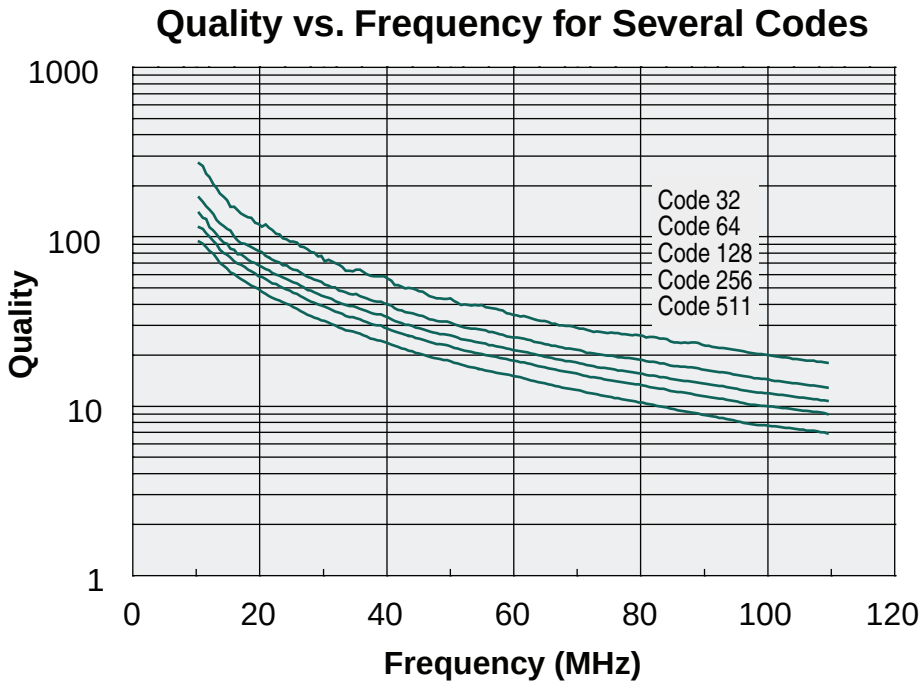


Figure 4: ESR vs. Code for Nominal Operation Conditions

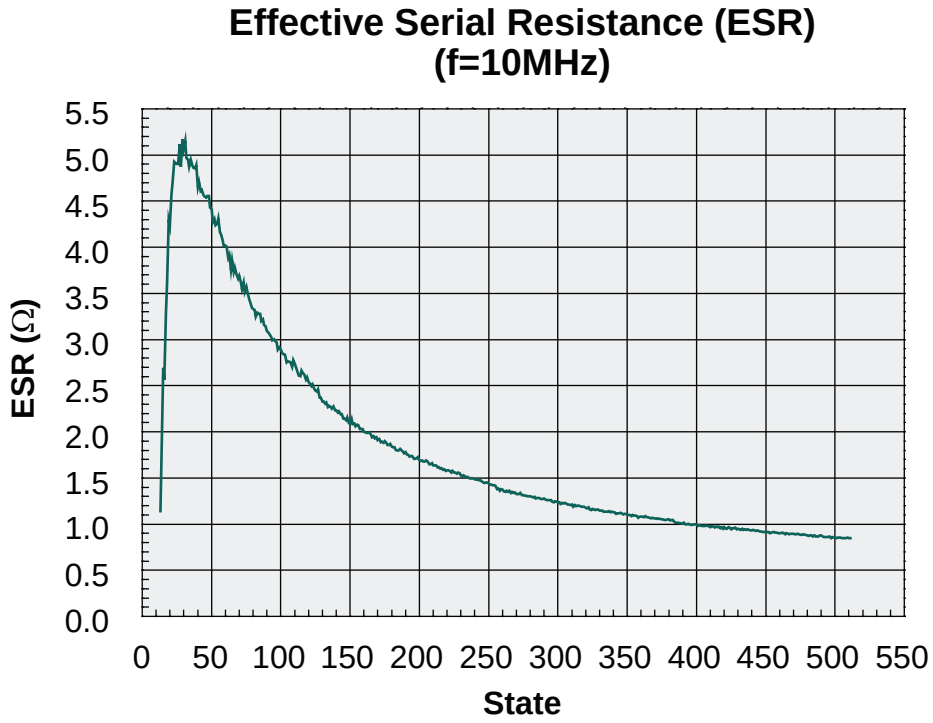
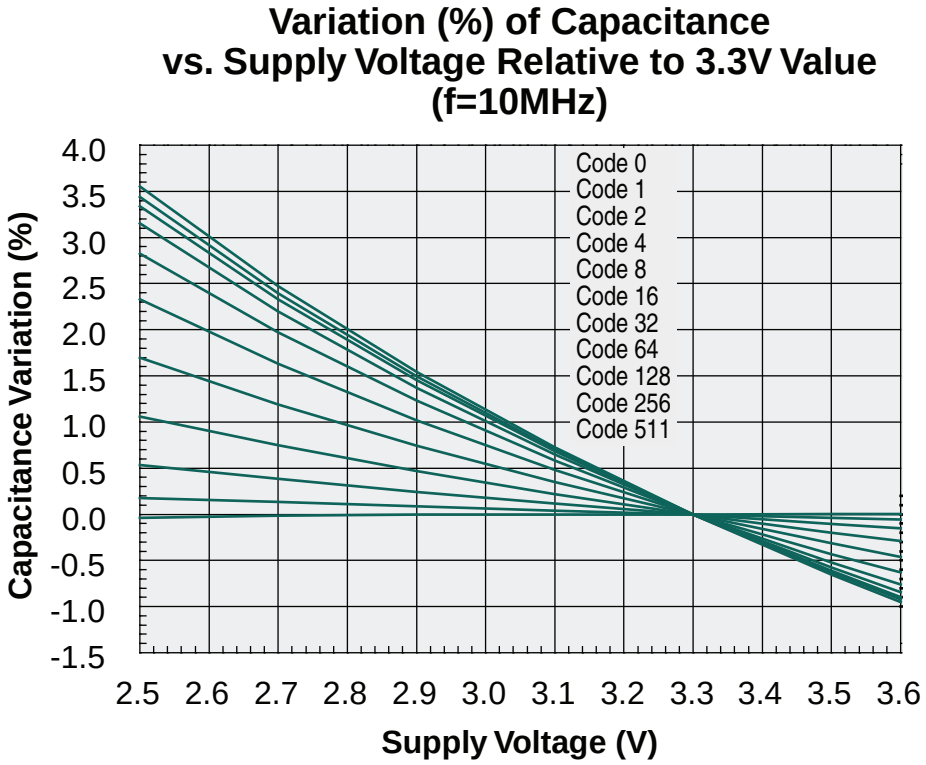


Figure 5: Variation of the Capacitance at 10MHz with Supply Voltage, Relative to the Value at 3.3V



The figure above shows how the equivalent capacitance varies with the supply voltage while CN is biased at half of the supply voltage level. Here, the value obtained for 3.3V is used as a reference and the deviation is given in percentage. Please note also that for supplies larger than 3.6V no further variations are expected.

The DC voltage biasing of the CN terminal has a small though visible influence on the performance of the Digital Programmable Capacitor. The table below presents the variation of the shunt capacitance and ESR at 10MHz when CN is biased at 0V, 1.65V and 3.3V.

	Capacitance (pF)			ESR (Ω)		
Code / V_{bias} (V)	0	1.65	3.3	0	1.65	3.3
0	1.7	1.7	1.9	0.509	0.442	0.695
1	2.1	2.1	2.3	0.739	0.720	1.006
2	2.5	2.5	2.7	0.949	0.973	1.29
4	3.2	3.2	3.5	1.271	1.366	1.742
8	4.7	4.7	5.1	1.754	1.952	2.431
16	7.6	7.7	8.2	2.256	2.564	3.188
32	13.7	13.7	14.3	4.342	4.968	6.31
64	25.6	25.6	26.4	3.259	3.755	4.882
128	49.6	49.6	50.3	2.063	2.372	3.14
256	97.4	97.5	98.1	1.204	1.377	1.827
511	193.2	194	193.2	0.75	0.846	1.106

For small variations of the supply voltage and CN biasing voltage around the 3.3V and, respectively, 1.65V nominal values, the following table can be used to estimate the deviation of the equivalent shunt capacitance. The effects of varying the two parameters are additive.

Relative deviation of the capacitance with supply and bias voltages around the nominal biasing point (pF/V)											
Parameter	Code 0	Code 1	Code 2	Code 4	Code 8	Code 16	Code 32	Code 64	Code 128	Code 256	Code 511
Supply (V)	-0.43	-0.43	-0.43	-0.42	-0.42	-0.41	-0.40	-0.37	-0.32	-0.21	0.01
Bias (V)	0.26	0.26	0.26	0.26	0.26	0.25	0.24	0.23	0.19	0.13	0

For example, for a deviation of +100mV in supply voltage and -100mV in CN bias voltage, the capacitance for code 0 will be modified by -0.069pF. Using the above-stated equation for calculating the nominal values of C_{SHUNT} or the next table with representative capacitance values, it can be expected that C_{SHUNT} is shifted from 12.5pF to 12.43pF.

3. Functional Description

3.1 Introduction

The NCD2400M provides a digitally controlled variable capacitance between pin CP and pin CN. This capacitance can be used as a series capacitance (between CP and CN) or shunt capacitance (connecting CN to GND).

The output capacitance is set either by the content of the volatile register or by the content stored in the non-volatile memory.

By default, the value of the capacitance at CP/CN is based on the digital value stored in non-volatile memory, but can be controlled directly with the content of the volatile register, depending on the operating mode indicated by the configuration register.

The load capacitance presented by the NCD2400M at pin CP/CN is defined by:

$C_{LOAD}=C_0+C_{var}$

Where:

- C_0 is the base load capacitance
- C_{var} is the tuning capacitance, controlled by the 9-bit control word

The NCD2400M has two operating modes related to the way the programmable capacitor is controlled (volatile register or non-volatile memory):

- Volatile Mode: the Control Data value loaded in volatile register determines the load capacitance
- Non-Volatile Mode (Default mode): the Control Data value written in the non-volatile memory determines the load capacitance

In Non-Volatile Mode, the default mode, the Control Data value is determined by the content of the non-volatile memory that was programmed earlier. Memory mode is applicable in situations in which the required output capacitance is unlikely to change and the control data must be retained across periods of no power.

Programming methods for the tuning capacitance are discussed below.

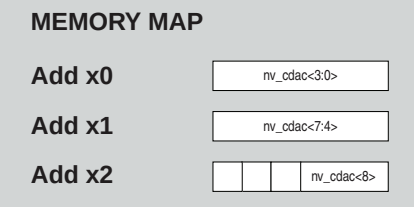
3.2 CDAC

The 9 bits in the Capacitive Digital to Analog Converter (CDAC) constitute the control bits of the capacitance tuning. The table below shows the expected capacitance values in series configuration for several codes, varying ±15% due to process variations.

Decimal	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	C_{LOAD} (pF)
0	0	0	0	0	0	0	0	0	0	1.7
1	0	0	0	0	0	0	0	0	1	2.1
2	0	0	0	0	0	0	0	1	0	2.5
3	0	0	0	0	0	0	0	1	1	2.9
4	0	0	0	0	0	0	1	0	0	3.2
5	0	0	0	0	0	0	1	0	1	3.6
6	0	0	0	0	0	0	1	1	0	4.0
7	0	0	0	0	0	0	1	1	1	4.4
125	0	0	1	1	1	1	1	0	1	48.6
126	0	0	1	1	1	1	1	1	0	48.9
127	0	0	1	1	1	1	1	1	1	49.3
128	0	1	0	0	0	0	0	0	0	49.6
250	0	1	1	1	1	1	0	1	0	95.3
251	0	1	1	1	1	1	0	1	1	95.7
252	0	1	1	1	1	1	1	0	0	96
253	0	1	1	1	1	1	1	0	1	96.5
254	0	1	1	1	1	1	1	1	0	96.8
255	0	1	1	1	1	1	1	1	1	97.2
256	1	0	0	0	0	0	0	0	0	97.5
499	1	1	1	1	1	0	0	1	1	188.7
500	1	1	1	1	1	0	1	0	0	189
501	1	1	1	1	1	0	1	0	1	189.4
502	1	1	1	1	1	0	1	1	0	189.7
503	1	1	1	1	1	0	1	1	1	190.2
504	1	1	1	1	1	1	0	0	0	190.4
505	1	1	1	1	1	1	0	0	1	190.9
506	1	1	1	1	1	1	0	1	0	191.2
507	1	1	1	1	1	1	0	1	1	191.7
508	1	1	1	1	1	1	1	0	0	192
509	1	1	1	1	1	1	1	0	1	192.4
510	1	1	1	1	1	1	1	1	0	192.8
511	1	1	1	1	1	1	1	1	1	193.2

3.3 Non-Volatile Memory Configuration

The non-volatile memory is organized in 3 words of 4 bits in length, as shown below:



3.4 Device Address

NCD2400M may have only two available addresses hard-coded during manufacturing. This is described in the table below.

Address Selection			
Model	Address (DEC)	Address (HEX)	Address (BIN)
NCD2400M-0	96	0x60	1100000
NCD2400M-1	97	0x61	1100001

This simple way of addressing allows for easy configuration in systems that employ up to two NCD2400M slaves.

3.5 Operating Modes

The NCD2400M functions in one of two different modes.

The load capacitance between CP and CN can be controlled by the value loaded into the volatile register, or by reading the value stored into the non-volatile memory.

By default, NCD2400M operates in Non-Volatile Mode so that in most end-user applications the capacitance value corresponds to the information programmed in the non-volatile memory.

Non-Volatile Mode is entered into automatically at power up, or after sending the "Change to Non Volatile Mode" command

Volatile Mode is entered into each time the Volatile register is written. This happens even if the NCD2400M has entered into the Non-Volatile Mode following a “Change to Non-Volatile Mode” command.

3.5.1 Volatile Mode

Volatile mode provides the means to alter the load capacitance at any time. The load capacitance value will be lost whenever power to the device is removed.

Because Volatile Mode is functional over the entire operational range of the NCD2400M, the capacitance presented between CP and CN can be modified under all acceptable operating conditions.

Modifying the capacitance is easily accomplished by writing the 9 bit control code into the volatile register, using the I^2C interface.

3.5.2 Non-Volatile Mode

Non-Volatile Mode is the default mode of operation. This operational mode uses the value stored in the non-volatile memory to configure the capacitor to the proper value.

There are internal pull up resistors (100kΩ nominal) at SDA and SCL pins to maintain inert logic '1' states at these inputs ensuring stable and predictable behavior without the need for supplementary external discrete components. This is especially useful in case these pins are left floating by customers who want to do one time programming, and don't need to change the capacitance value of NCD2400M during normal operation.

3.6 I^2C: Serial Interface Operation

The NCD2400M digitally controlled variable capacitor can be accessed using an I^2C serial interface. The NCD2400M can only act as a Bus Slave. The Bus Master initiates the start of serial transaction by driving SDA (Serial Data) low while SCL (Serial Clock) remains high. Each bit of the telegram is clocked in on the rising edge of SCL. Transitions on SDA are allowed only when SCL is low. The NCD2400M activates the acknowledgement bit following each data word so that it can be clocked in by the host on the rising edge of SCL.

Depending on the value of the R/W bit after sending the device address, the write or read operation will be chosen.

Four operations are available through this Serial Interface: “Write Volatile Register Operation”, “Write Non-Volatile Memory Operation”, “Read Operation” and “Change to Non-Volatile Mode”.

3.6.1 Write Operation

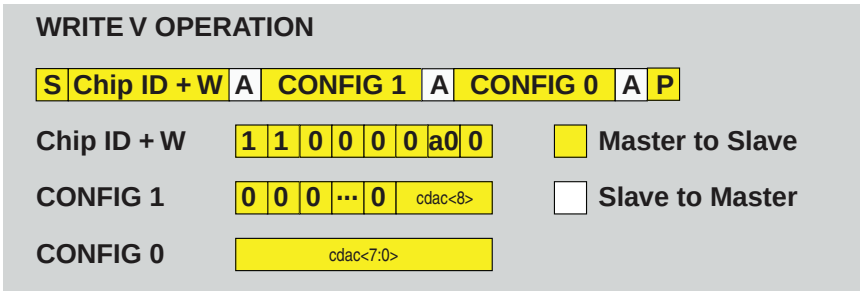
If the Device Address is considered valid and the R/W flag is set to 0, then the device will execute a Write Operation. Following the Device Address block, the Master will send two “Config Byte” sequences. (“CONFIG 1” and “CONFIG 0”).

Both “CONFIG 1” and “CONFIG 0” contain 8-bit words. The first bit from the “CONFIG 1” block, determines whether to write in the Volatile Register or in the Non-Volatile Memory.

Write Volatile Register

Timing diagram for writing Volatile register is shown below. V/NV set to '0' determines the writing into the Volatile Register. The data to be written is sent encoded within two Configuration Byte blocks as such:

- The last bit of “CONFIG 1” is cdac<8>
- “CONFIG 0” represents cdac<7:0>



Write Non-Volatile Memory

Non-volatile memory is programmed a word for each command. Furthermore, each block must be erased before being written.

Timing diagram for this operation is shown below. V/NV (first bit of CONFIG 1) set to '1' determines the writing into the Non-Volatile Memory.

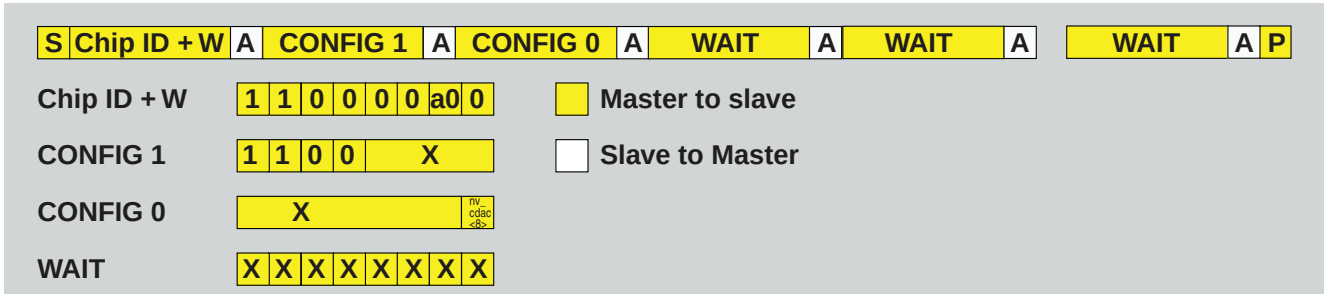
The data to be written is sent encoded within two Configuration Byte blocks as shown in the table below.

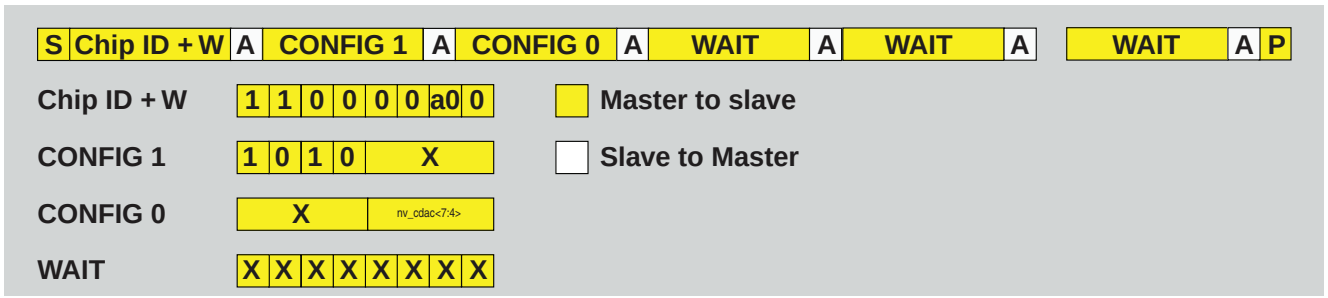
CONFIG 1	CONFIG 0
1100xxxx	xxxxxxx nv_cdac<8>
1010xxxx	xxxx nv_cdac<7:4>
1000xxxx	xxxx nv_cdac<3:0>

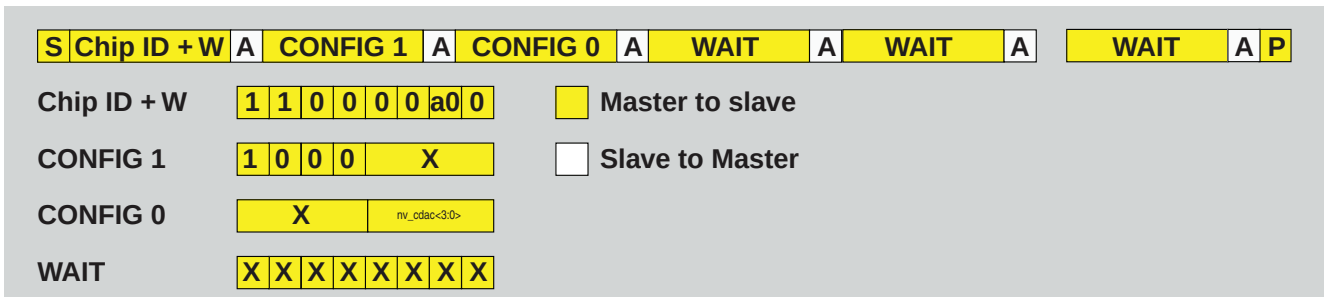
The write pulse duration is controlled by the Master by sending a determined number of empty blocks depending on the I^2C clock frequency.

The erase operation is a normal write command, with nv_cdac set to '0'.

WRITE NV OPERATION





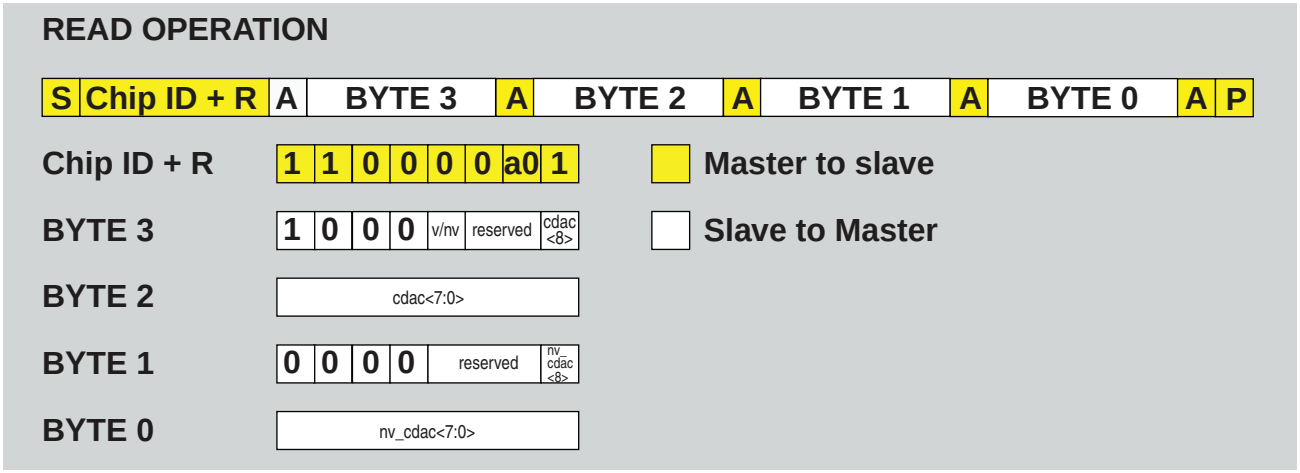


3.6.2 Read Operation

If the Device Address is considered valid and the R/W flag is set to 1, then the device will execute a Read Operation. Following the Device Address block, the slave device will answer with 4 other bytes, specified as follows:

- "BYTE 3" contains the current Operating Mode ('0' Volatile, '1' Non Volatile), some reserved bits and cdac<8>
- "BYTE 2" contains cdac<7:0>
- "BYTE 1" contains some reserved bits, and nv_cdac<8>
- "BYTE 0" contains nv_cdac<7:0>.

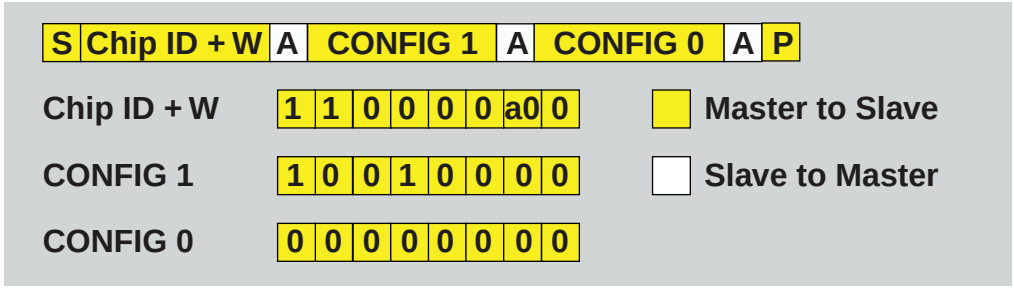
Timing diagram is shown below.



3.6.3 Change to Non-Volatile Mode

If the Device Address is considered valid, the R/W flag is set to 0, and the first and fourth bits of CONFIG1 are set to 1, then the device will change to Non-Volatile Mode. Once this operation is executed, the output capacitance value will be updated with the value stored in the Non-Volatile Memory.

Timing diagram is shown below.



3.6.4 Programming the Non-Volatile Memory

The electrical and timing conditions that must be followed for reliable programming are shown below.

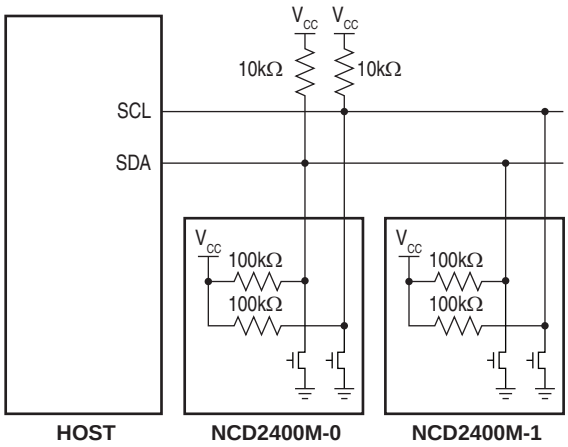
Non-Volatile Memory Programming Conditions

The NCD2400M must be programmed or configured under following conditions:

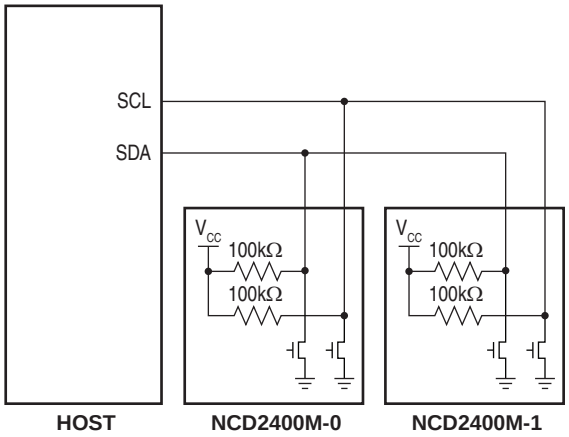
- Clock: F_{SCL}=max. 400kHz
- Clock: D_{SCL}=50% ± 10%
- Programming pulse duration is 5ms typical; to be controlled by the Master depending on SCL frequency.

3.8 Application diagram

The recommended application diagram for the I^2C communication from the Host (master), to two NCD2400M devices, operating as slaves, is shown in the picture below. In general, it is recommended to use 10kΩ pull-up resistors in both lines, SDA and SCL. This is more important if there are more slave devices connected to the lines, or if the interconnection lines in the PCB are long.



For some specific applications, in which there are no other slave elements connected to the lines, and in which the parasitic capacitances of the interconnection lines are low (few pF), users might try to avoid external pull-up resistors, using the internal pull-up resistors instead.



4. Load Capacitance Programming Procedure

Full configuration of NCD2400M for users who want to address up to 2 devices with the same host and who want to use the Memory mode for capacitance control is described below. These are the phases:

- Capacitance Trim Code Determination
- Capacitance Trim Code Programming

The capacitance of each of the used devices can be trimmed using the Volatile Register in order to make trials until the right code to be programmed is found. This step is recommended for all users. After that, the code can be programmed in the Non-Volatile Memory. Memory is erased before being written in order to delete any old content. For instance, this is the sequence to write capacitance codes 0x125, 0x126 and 0x127, finally programming 0x127 inside device with address 0x60.

- Write 0x125 into the Volatile Register of the Device Address 0x60.
- Write 0x126 into the Volatile Register of the Device Address 0x60.
- Write 0x127 into the Volatile Register of the Device Address 0x60.
- Write 0x127 into non-volatile memory address of Device Address 0x60 using following sequence:
  - Erase (Write 0x0) into non-volatile memory address 0h of Device Address 0x60
  - Write 0x7 into non-volatile memory address 0x0 of Device Address 0x60
  - Erase (Write 0x0) into non-volatile memory address 0x1 of Device Address 0x60
  - Write 0x2 into non-volatile memory address 0x1 of Device Address 0x60
  - Erase (Write 0x0) into non-volatile memory address 0x2 of Device Address 0x60
  - Write 0x1 into non-volatile memory address 0x2 of Device Address 0x60
- Read the memory content using the Read command. Note that the capacitance won't change and will correspond to the content of the Volatile Register, unless the mode is changed to Non-Volatile.
- Change to Non-Volatile mode

Different sequences than the one described above, such as erasing all blocks before writing them, are also possible.

5. Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
NCD2400M	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

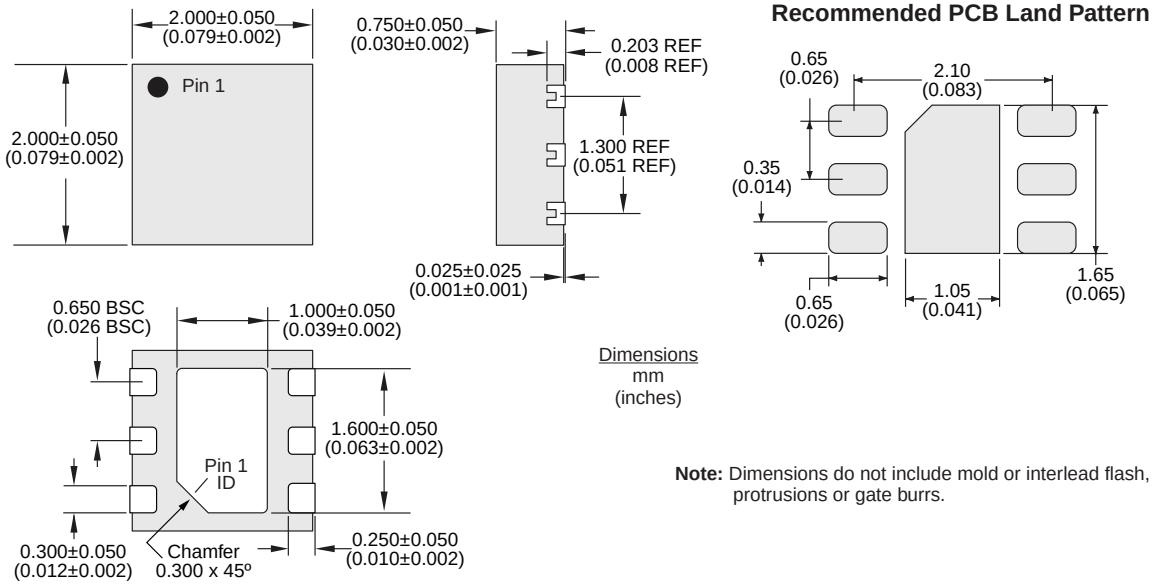
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
NCD2400M	260°C	30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

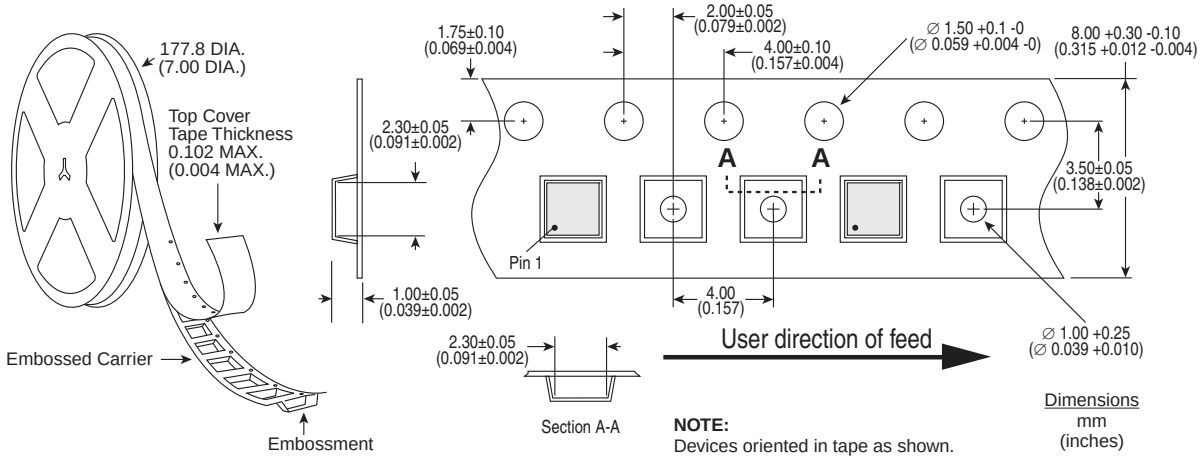
5.5 Mechanical Dimensions

5.5.1 NCD2400M DFN-6 Package Dimensions



Note: Dimensions do not include mold or interlead flash, protrusions or gate burrs.

5.5.2 NCD2400MTR DFN-6 Tape & Reel Specification



NOTE:
Devices oriented in tape as shown.

For additional information please visit www.ixysic.com

Specifications: DS-NCD2400M-R00B

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